REMARKS

The rejection of claims 68, 71, 78, 85 and 86, 92 and 94 and 95, under 35 U.S.C. §112, second paragraph, is respectfully traversed.

Claim 68 is amended to particularly claim the symmetrical nature of the device. The limitation "zero bottom width" implies a curved device.

Claim 71 is amended by deleting the phrase through a curvature-related stress-relieving and strain-relieving mechanism", and clarifying language is added.

Claim 78 is amended by deleting the phrase "and being uniformly bonded uniformly to at least a selected area of the substrate avoiding imperfectly bonding interfacial region"and clarifying language is added.

Claim 85 is amended by deleting the phrase "being reduced but not eliminated, through a curvature-related strain-relieving and stress-relieving mechanism operating on the curved adjoining surface" and clarifying language is added.

Claim 86 is amended by deleting the phrase "the PN junction region is within 40 atomic layers from the substrate ; and

the stresses and strains are reduced, but not completely eliminated, by a curvature-related stress-relieving mechanism; and

the remaining stresses and strains still provide sufficient stresses and strains to favorably affect characteristics of the PN junction region" and clarifying language is added.

Claim 92 is amended by deleting the phrase " [through a curvature-related strain-relieving and stress-relieving mechanism".

Claim 94 is amended by deleting the phrase and

the solid state material layer is mechanically perfect and is no more than 3 to 40 Angstroms thick."

Claim 95 is amended by deleting the phrase " with a mechanically perfect bonding interfacial region to avoid imperfectly bonded material layer leading to poor device yield, performance, reproducibility, reliability, and life."

In view of the above amendments, applicant submits that the rejection of claims 68, 71, 78 85 and 86 92 and 94 and 95, under 35 U.S.C. §112, second paragraph, is overcome.

The rejection of claims 67, 69 70, 72-79, 81, 84-88 and 93-95 under 35 U.S.C. §103 over Li, US Patent No. 5,696,402 is respectfully traversed.

The PN junction region is disclosed in the '402 patent as being 1 micron thick. See, e.g., Col. 7, line 25. This 1-micron thick junction region, (10,000 angstroms), is **2,000 to 200** times thicker than the solid state material layer 44, 47, or 51-54 of the presently claimed invention.

According to Moore's law, familiar to the skilled artisan, it takes about 18 months (one and half years) to half a device feature size. Hence, to reduce the gate or field layer thickness by orders of magnitude from 1 micron (10,000 Angstroms) to 10 Angstroms requires many years, and thousands of the world's top scientists and engineers, and billions of dollars in equipment, salaries, and materials. Certainly, such size reductions in the semiconductor industry are remarkable quantum jumps, rather than mere differences in degree.

As a matter of fact, the semiconductor industry across the entire world is trying to achieve the size reduction herein claimed; however, the industry has not achieved the

results herein achieved. After spending many years and many billions of dollars, no one has o been able to reduce the gate layer thickness from, e.g., 20 Angstroms thick to 10 or even 15 Angstroms thick.

Further, each device of the '402 patent requires five (5) essential or critical elements. If any one of these critical elements of the '402 device is absent the claimed device will not work. These elements are:

a) Subgroove 18;

b) radius of curvature r for subgroove 18;

c) groove 14;

d) radius of curvature r_1 for subgroove 14; and

e) R_2 must be significantly greater than (claim 1 of '402), at least twice greater than (claim 2 of '402), or 1-4 orders of magnitude greater than r_1.

The claims of instant '874 application, do not require any one of the five critical or essential elements of the '402 patent. Even the first claim element of the '402 patent, the subgroove 18, is not recited, because claims in this invention require only one single, totally different element, i.e., "a solid state material layer less than 10 Angstroms thick" (e.g., claim 66, line 3). This is not even a single submicron "subgroove 18". In patent terms, a submicron "subgroove" is simply not "a solid state material layer less than 10 Angstroms thick" or "one atomic layer thick".

Further, the grooves of '402, being possibly filled with gas, such as air, nitrogen, or vacuum, certainly cannot be "metallurgically bonded" to the silicon sides of the groove. There simply is no metal, nor any solid, to be bonded to the silicon substrate or body.

In addition, the "in-situ" oxidation of the silicon to form the oxide or nitride gate layer is extremely non-uniform and superficial, to the extent of only about 18

Angstroms. This cannot produce the "solid state material layer" of the present invention. There can be little formative volume expansion that produces any appreciable "beneficial residual compressive stresses" in the silicon. Also, the groove always has the usual "voids, porosities, microcracks, faults, and other defects" in the prior-art solid groove materials. These defect prior-art groove materials can be very damaging and non-beneficial, and contain fatal defects.

Hence, the applicant respectively submits that the '402 patent does not teach, or suggest the "solid state material layer less than 10 Angstroms thick" of the claimed invention. The two inventions are patentably distinct and different from each other, not because different words are being used to describe the same structure. In particular, the mechanically perfect solid state material layer of 10 Angstroms of the claimed invention does not and cannot describe the much broader but different submicron subgroove 18 of the 402 patent. Even if we assume the submicron subgroove of the '402 patent to be the "solid state material layer" of the claimed invention, the submicron thickness of the subgroove 18 differs, by orders of magnitude, in size from the solid state material.

Additional differences between the present invention and the '402 invention include:

1) The '402 patent deals with "radius of curvatures", while this invention deals with thickness;

2) The '402 device requires two (2) curvatures, both less than 1 cm (100,000,000 Angstroms) in radius of curvature. Further, one radius of curvature must be significantly greater than the other (claim 1), at least two times greater (claim 2), or 1-4 orders of magnitude greater (claim 9), than the other radius of curvature. The smaller radius must still be some 5,000 Angstroms in size. These numbers are still orders of magnitude greater than the thickness, not radius, of the present invention;

3) The present invention can have a curved layer, but need not be curved, e.g., in the flat gate layers Even with a curved gate layer, there need only be one curvature,

or at least only one continuous, smooth curve, rather than one with two abrupt transitions at the two left and right edges of the top of the smaller curve 18 as in the '402 patent;

4) The PN junction layer in '402 is the closest "layer" to material layers of the present invention. But the PN junction layer consists of a semiconductor material and is, therefore, electrically conductive at least part of the time, i.e., forward-biased. In contrast, the solid state material layer of this invention, whether a field or gate layer, is not a semiconductor, or eutectic melt-formed material in '406, but is a non-eutectically formed, non-conductive, non-semiconductor, non-metallic material, and non-eutectic material, but an electrically insulating material, such as SiO_2, which is electrically insulating at all times; and

5) The PN junction layer in '402 has a totally different structure, mode of operation, and result compared to the solid state material layer of the present invention.

In view of the above, applicant respectfully submits that the rejection is made in error and should be withdrawn.

The rejection of claims 66, 80, 82-83, and 89-91 under 35 U.S.C 103(a) as being unpatentable over Li, U.S. Patent No. 4,371,406 is respectfully traversed.

Like above the above discussed deficiencies of the '402 patent, the '406 patent also fails to disclose a "solid state material layer" which is less than 10 Angstroms or even one atomic layer thick.

Perhaps the Office has taken the eutectically grown (col. 4, lines 32-34) p-type semiconductor, n-type semiconductor, PN junction region layers of Li as the "solid state material layers" of the claimed invention. All three of these semiconductor materials layers contain substantial amounts of metals. These amounts are not in the ppm or

ppb trace amounts range of dopant metals. The metals used in the eutectic matrix of the '406 devices include: Ag, Al, Au, Bi, Ga, In, Pb, Sb, S.n., Tl, and Zn with Ge eutectic devices; and Ag, Al, Au, Be, Ga, In, Sb, S.n., As, Ca, Ce, Co, Cr, Cu, Fe, Mg, Mn, Mo, Nb, Ni, Pd, Pt, Ta, Ti, U, V, and W, and Zr with Si eutectic devices (See '406 col. 5, line 68 to col. 6, line 1; and col. 6, lines 7-10). These are not semiconductor and certainly not the insulating oxide/nitride material of the solid state material of the materials of the present invention.

The eutectic matrix and phase body materials have orders of magnitude different thermal and electrical conductivities and thermal expansion coefficients, and widely different melting points relative to those of the "pocket" and "substrate" of the present invention. The "substrate" and "pocket" of the '406 devices are metal-containing eutectically melt-grown eutectic phase bodies having entirely different thermal and electrical conductivities, thermal expansion coefficients, melting points relative to the "body" and "substrate" of the '406 devices.

The p-type, n-type, and PN junction layers in '402 and '406 are semiconductors. They are electrically conductive at least part of the time, i.e., forward-biased. In contrast, the solid state material layer of this invention, such as silicon dioxide, is an electrical insulator. Whether used as a field or gate layer, it is not an electrical conductor under all conditions of electrical bias; and

Hence, the PN junction layer in '402 and '406 has a totally different structure, mode of operation, and result compared to the solid state material layer of the present invention.

In addition and most importantly, the eutectic phase bodies, though "microscopic", are still over **fractional micron to 15 microns** in thickness (col. 4, line 36-37), or still some 400 to 80 times thicker than the thickness of the solid state material layer of the claimed invention. Again, it would take many years and many

billions of dollars to reduce the '406 device sizes to those of the present invention, according to Moore's law.

The '406 patent did disclose the possibility of growing "smaller eutectic sheet thickness are possible, but only under high growth rates, small temperature gradients in the liquid, and high impurity concentration in the melt. But the growth interfaces are unstable. No useful eutectic device phase bodies then result because of growth breakdowns" ('406 in col. 14, lines 8-42). This is an extremely tough problem even more difficult than the universally unsolvable thin gate layer problem.

Nor does "atomically smooth major surface" of claim 93, line 5 exist in '406 devices. The '406 patent discloses "microscopic" (Col. 4, line34) "eutectic" (col. 4, line 32) "sheet phase bodies" (col. 4, line 34). But Col. 4, lines 36-37 disclose that "By microscopic, I mean fractional microns to about 15 microns in thickness." Fractional microns are several hundred times larger than the "10 Angstroms" thickness in the instant application. According to the Moore's Law, it takes 18 months (one and half years) to half the device size. From submicron to 10 Angstroms would thus require about 14 years and tens of thousands of top scientists and engineers, plus many billions of dollars of investment in equipment, materials, and research and development.

Further, due to the presence of submicron objects, such as subgroove 18 in the '402 patent and the eutectic phase bodies in the '406 patent, the "solid sate material layer" cannot possibly have typically 10 angstroms of thickness, surface smoothness and accuracy of thickness or smoothness.

In addition, the devices in '406 are eutectic (col. 4, line 32) devices of a semiconductor (e.g., Si or Ge) and a metal (e.g., col. 6, line 67 to col. 6, line 10). Having eutectic compositions and properties, and melting at much lower eutectic temperatures, "the eutectics from these melts contain microscopic, metallic phase

bodies which, being in intimate contact with the semiconductor Ge or Si bodies, are ... useful as ... multiple ohmic or metal-semiconductor barriers." (Col. 6, lines 3-7).

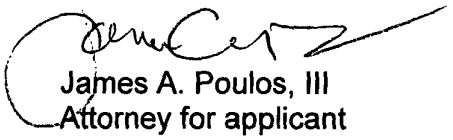
Therefore, the integrated circuits of '874 have unique, entirely different structures, modes of operation, and results over prior-art devices.

Hence, the rejection of claims 66, 80, 82-83, and 89-91 based on 35 U.S.C.103(a) as being unpatentable over U.S. Patent No. 4,371,406 is improper and should be withdrawn.

In view of the amendments and remarks above, Applicants submit that this application is in condition for allowance and request reconsideration and favorable action thereon.

Any fee not covered and required for entry of this amendment should be charged to the undersign's deposit account 50-1770.

Respectfully submitted,



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Enclosures: substitute pages 17 and 29
Drawing changes Figs 1-3
EOT (2)
IDS and 8 citatiations

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

Otherwise referred to as the Paper Proliferation Act

Applicant is providing a new substitute page 17 of the specification. Reference to Fig 6 is deleted in this substitute page in addition a substitute page 29 is provided changing "43"in lien 19 to --48--.

The claims are amended as shown below

--66. A solid state device comprising:

a solid state material substrate having a top surface; and

a solid state material layer no more than [3 to 40] 10 Angstroms thick[, having at least one smooth major surface,] and positioned on the top surface of the substrate;

at least a portion of the solid state material layer being metallurgically [perfectly] bonded [uniformly] to [the] at least a selected portion of the [solid state device] top surface of the solid material state substrate [achieving thermochemical stability of a bonding interfacial region].

67. A solid state device as in claim 66 in which the solid state material layer has at least [a number] two of the following features: a) having an atomically smoothed bottom surface; b) having a curved top surface; c) having an atomically liquid-smoothed gate bottom layer; [c] d) made of purified material; [d] e) made of strengthened material; [e] f) accurate to one atomic layer in thickness; [f] g) aged by liquid diffusion; [f] i) fine-grained or subgrained; [h] j) oriented grains or subgrains;[i] k) narrow grains or subgrains; and [j] l) stronger than unbonded material[; the number being selected from the group consisting of one, two, and three].

68. The device as in claim 66 in which the solid state material layer has a central portion of zero bottom width which is symmetrical with respect to a central vertical bisecting plane thereof [whereby no weaker side exists].

69. The device as in claim 66 in which the solid state material layer [is formed using real-time monitoring and closed-loop feedback control to achieve a precision of one to] has an accuracy of better than several atoms on a [material] layer dimension selected from the group consisting of thickness, depth, curvature, shape, size, chemical composition profiling, and lateral location.

70. The device as in claim 66 in which at least a portion of the solid state material layer contains [is bonded to the substrate with an initially liquid bonding material;

the liquid bonding material wetting and filling surface defects on the solid state material layer and then solidifying and converting these liquid-filled surface defects into]

solid reinforcements, whereby the bonded material layer is stronger than the unbonded solid state material itself.

71. The device as in claim 66 in which the solid state material layer is sufficiently thin and flexible so as to yield under stress [significantly thereby] preventing device failure [failures through a curvature-related stress-relieving and strain-relieving mechanism].

72. The device as in claim 66 in which the solid state material layer is [formed at least partly by laser heating to melt the solid state material layer; and including controllably solidifying the melted layer material into a] liquid-diffusion aged [, solid state material layer].

73. The device as in claim 66 having a thickness of less than a micron [one atomic layer] thereby forming a thin-film integrated circuit device.

74. The device as in claim 66 wherein the solid state material layer [is] has a curved major surface with a radius of curvature of less than [a value selected from the group consisting of 0.5 microns and] 1 micron.

75. The device as in claim 66 in which material of the solid state material layer is [made] purified by a melting and solidification process;

the purity of material of the solid state material layer being improved [due to the melting and solidification] by at least one order of magnitude [based] relative to the solid state material prior to said metallurgically bonding [on a segregation coefficient according to a relevant alloy phase diagram].

76. The device as in claim 66 in which the solid state material layer has [at least] an accuracy in thickness of one atomic layer [atomically smooth major surface produced by an atomic smoothing process].

77. The device as in claim 66 in which the solid state material layer comprises an ion implanted region with [is made by ion implantation under 1 kilovolt of implanting voltage to achieve] a depth accurate to several atomic layers .

78. A solid state device as in claim 66 including:

[a] first and [a] second solid state material pockets positioned adjacent to each other, but laterally separated by a gap, on the top surface of the substrate;

the solid state material layer [thereby] filling and bridging the gap between the two adjacent solid state material pockets; and

at least a portion of the solid state material layer having an accuracy in thickness of [no more] better than three atomic layers [and being uniformly bonded uniformly to at least a selected area of the substrate avoiding imperfectly bonding interfacial region].

79. A solid state device as in claim 78 in which:

at least a part of the substrate is a semiconductor of a first conductivity type; and

at least one of the semiconductor pockets is of a second conductivity type forming at least one PN junction region where the part of the substrate contacts the at least one semiconductor material pocket.

80. The device as in claim 66 in which the solid state material layer is selected from the group consisting of a gate layer and a field layer.

81. The device as in claim 66 in which the substrate material is selected from the group consisting of Si, Ge, Si-Ge, InP, InSb, GaAs, SiC, InAs, superconductor, diamond, semiconductor material, intrinsic semiconductor material, substantially electrically insulating material, and substantially electrically conducting material, and mixture thereof.

82. The device as in claim 66 selected from the group consisting of metal-oxide-semiconductor (MOS) device, [and] conductor-insulator-semiconductor (CIS) device, thin-film integrated circuit, and flexible integrated circuit.

83. The device as in claim [66] 78 in which:

the first and second solid state material pockets are respectively source and drain semiconductor pockets in a CMOS device and separated by a gap from each other; the solid state material layer is a gate layer filling and bridging the gap between the two pockets; and

the gate layer material [is laser heated and melted to smooth] has an atomically smooth surface at least on one of the top and major bottom surfaces thereof [by an atomic surface-smoothing mechanism; and

solidification of the molten gate layer material, sub-layer by sub-layer from the bottom surface up, purifies the gate layer material greatly reducing impurities and improving insulation most at a surface contacting the substrate].

84. The device as in claim [66] 83 in which [at least] each of a major portion of the substrate, solid state material pockets, and solid state material layer[, and electrical contacts are selected to consist] consists essentially of a single [intrinsic] doped and less doped intrinsic semiconductor material whereby the device is made resistant to dynamic forces due to impacts, vibrations, and large and rapid accelerations and decelerations[, because the plurality of the selected device component materials have practically the same density and differ from each other by only ppm or ppb of impurities].

85. The device as in claim 66 including a PN junction region having a curved adjoining surface [and provided on] contacting the substrate[; and] to thereby reduce but not eliminate at least one of inevitable thermal mismatch stress and in situ volume

change strain generated during device processing [being reduced but not eliminated, through a curvature-related strain-relieving and stress-relieving mechanism operating on the curved adjoining surface]

the remaining residual strain and stress on the curved adjoining surface of the PN junction region [being utilized to improve] improving a selected device performance.

86. The device as in claim 79 in which:

[the substrate is a semiconductor of one conductivity type and has a matching part contacting the curved adjoining surface of] the at least one PN junction region has a curved adjoing surface;and

the at least one of the first and second solid state material pockets [is a semiconductor of the opposite conductivity type thereby forming at least one PN junction region where the substrate] meets the curved adjoining portion of the at least one PN junction region [solid state material pocket;

the PN junction region is within 40 atomic layers from the substrate ; and

the stresses and strains are reduced, but not completely eliminated, by a curvature-related stress-relieving mechanism; and

the remaining stresses and strains still provide sufficient stresses and strains to favorably affect characteristics of the PN junction region].

87. The device as in claim 66 in which the solid state material layer has [been superficially ion-implanted with dopants in high concentrations therein;

the superficially ion-implanted layer being rapidly laser spike melted to have superficial liquidisation and a very] a shallow, highly activated doped region [due to the high spike heating rates allowing] having much greater dopant concentrations than the thermal equilibrium phase-diagram values.

88. The device as in claim 66 in which the solid state material layer is an electrically insulating, wavy and curved field layer [formed by at least partly ion-implanting with an ion-implanting beam into a silicon material substrate] containing an ion-implanted [a] substance selected from the group consisting of oxygen and nitrogen[;

at least one of the substrate and the ion-implanting beam having a wavy and curved movement relative to the other during the ion-implanting process to produce the wavy and curved field layer].

89. The device as in claim [66] 78 in which:

the first and second solid state material pockets are respectively source and drain semiconductor pockets in a CMOS device; [and]

the solid state material layer is a gate layer [bridging the gap between the two pockets]; and

including a conductive gate electrode [formed] of an electrically conducting material [and generally centered on the gate layer] to control flow of electronic carriers from the source to the drain.

90. The device as in claim 89 in which:

[a laser heating beam melts] the gate layer material [and smooths] is atomically smoothed on at least one of top and bottom major surfaces thereof [by an atomic surface-smoothing mechanism achieving] to achieve maximum smoothness; and

[solidification of] material of the [molten] gate layer being most purified [material, sub-layer by sub-layer from the bottom surface up, purifies the gate layer material greatly reducing impurities and improving insulation most at the] at a bottom surface facing the substrate.

91. The solid state device as in claim 66 in which:

the solid state material layer is a field layer separating and electrically isolating device components from each other;

the field layer on a horizontal cross-section thereof has a plurality of curved sections; and

each curved section has an arc length defined by: $l = r \times A$ where l is the arc length, r is the radius of curvature of the arc, and A is the subtended arc angle;

each arc section being capable of flexing whereby the arc length is changed by $\text{delta } l = r \times \text{delta } A + A \times \text{delta } r$; and

the changes in delta l, delta r, and delta A all being in directions to reduce thermal mismatch strain and automatically stopping when the residual thermal mismatch strain is reduced by the changing arc length to a point such that the multiply curved field layer can tolerate without failure the residual thermal mismatch strain.

92. The solid state device as in claim 66 in which the solid state material layer is curved to minimize thermal mismatch stresses [through a curvature-related strain-relieving and stress-relieving mechanism].

93. A mass-produced solid state device comprising:

a solid state material substrate;

at least one first solid state material pocket positioned on a first selected surface of the substrate; and

a solid state material layer having at least one atomically smooth major surface which contacts and metallurgically [perfectly] bonds [uniformly] the first selected surface of the substrate to a first specified portion of the at least one first solid state material pocket.

94. A solid state device as in claim 93 further comprising:

a second solid state material pocket positioned on a second selected surface of the substrate, and laterally adjacent to, but separated by a gap from, the at least one first solid state material pocket; and in which:

the solid state material layer fills the gap between the two material pockets while contacts and metallurgically [perfectly] bonds [uniformly] with a second specified portion of the second solid state material pocket[; and

the solid state material layer is mechanically perfect and is no more than 3 to 40 Angstroms thick].

95. A mass-produced solid state device comprising:

a solid state material substrate;

a left and a right adjacent solid state material pockets laterally separated by a gap and positioned on a common top surface of the substrate;

a curved solid state material layer which: a) [has a radius of curvature of no more than 1.0 micron] is less than 40 angstroms ; and b) is positioned on the top surface of the substrate to bridge the gap between the two solid state material pocket[; and

at least a portion of the solid state material layer being metallurgically continuously bonded to at least a selected area of the top surface of the substrate with a mechanically perfect bonding interfacial region to avoid imperfectly bonded material layer leading to poor device yield, performance, reproducibility, reliability, and life].